**Given:**

Processor Address Size: 32 bits

Cache Size: 16 KB (16 \* 1024 = 16,384 bytes)

Associativity: 4-way

Line Size: 4 words × 32 bits = 4 × 4 bytes = *16 bytes per line*

**Solution:**

1. Calculate Number of Cache Lines

Cache size = 16 KB = 16,384 bytes

Each cache line = 16 bytes

Number of lines = 16,384 / 16 = *1024 lines*

2. Determine Number of Sets

Since it’s a 4-way set associative cache, there are:

Number of sets = 1024 lines / 4 ways = *256 sets*.

3. Breakdown of 32-bit Address

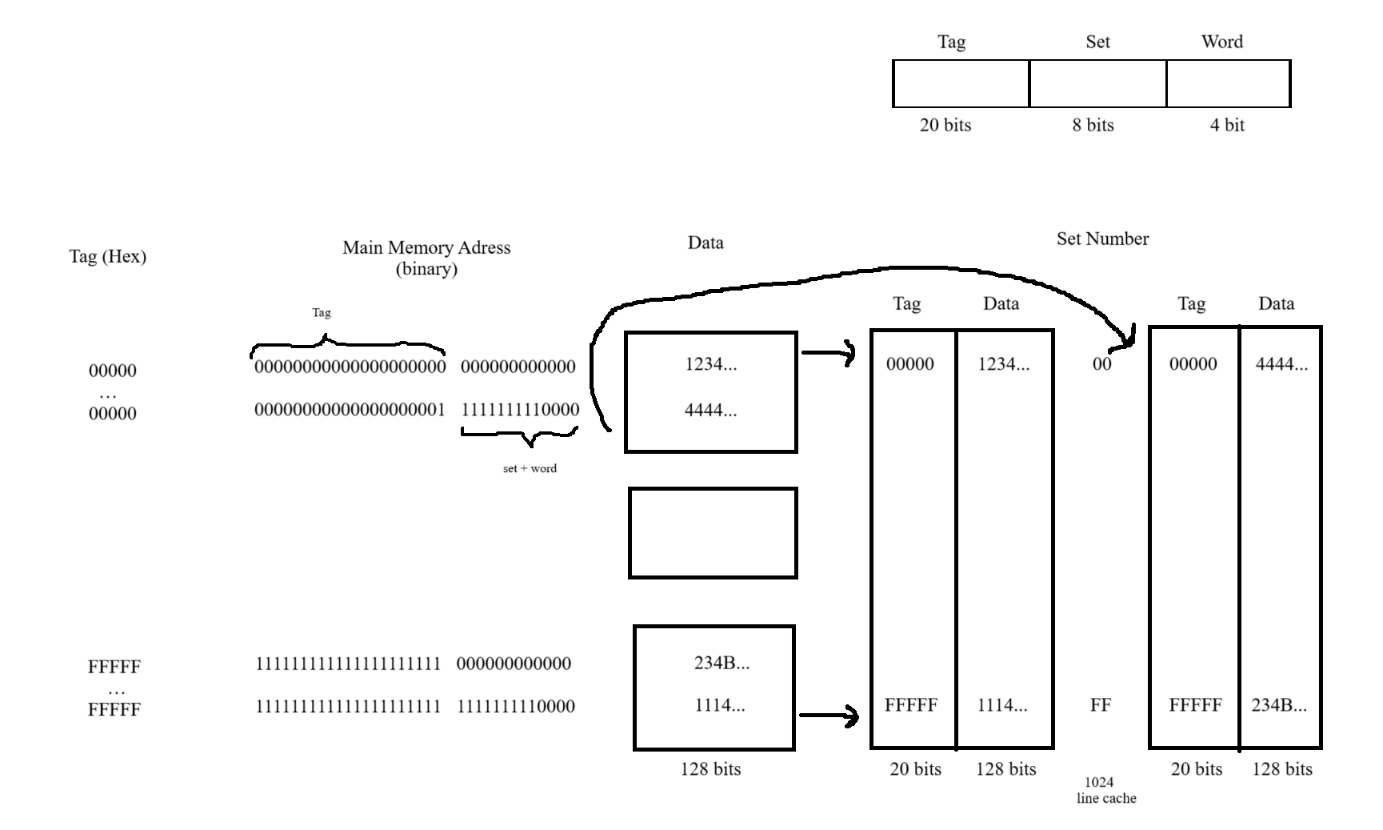
To map memory addresses to cache, divide the 32-bit address into:

**Word Offset:** 16 bytes per block = 2 + 4 ⇒ *4 bits for block offset*

**Set Index:** 256 sets = 2^8 ⇒ *8 bits for set index*

**Tag:** 32 − (4 + 8) = *20 bits for tag*

**Diagram:**

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